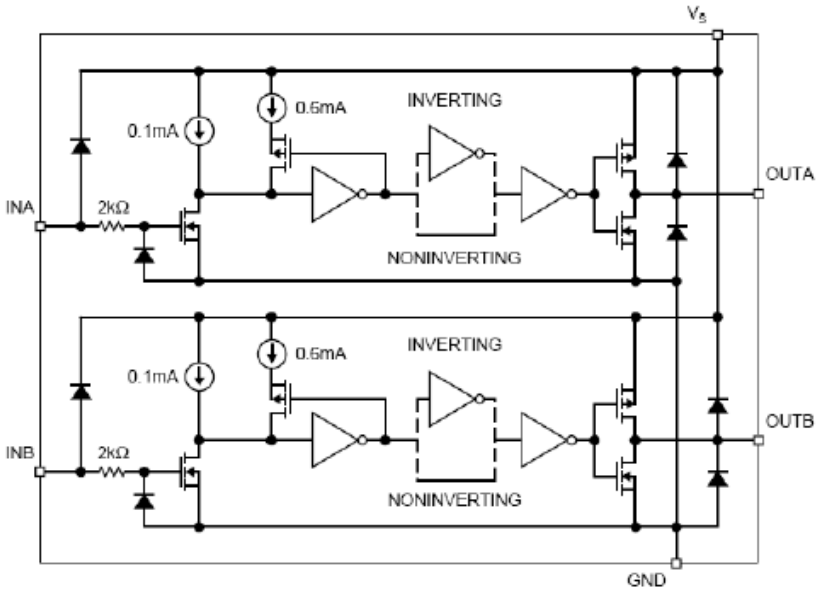
Features

- Bipolar/CMOS/DMOS construction
- Latch-up protection to >500mA reverse current
- 1.5A-peak output current
- 4.5V to 18V operating range
- Low quiescent supply current
  4mA at logic 1 input
  400uA at logic 0 input
- Switches 1000pF in 25ns
- Matched rise and fall times
- 7Ω output impedance
- <40ns typical delay
- Logic-input threshold independent of supply voltage
- Logic-input protection to -5V
- 6pF typical equivalent input capacitance
- 25mV max. output offset from supply or ground
- Dual inverting, dual noninverting, and inverting/noninverting configurations
- ESD protection

Functional Diagram



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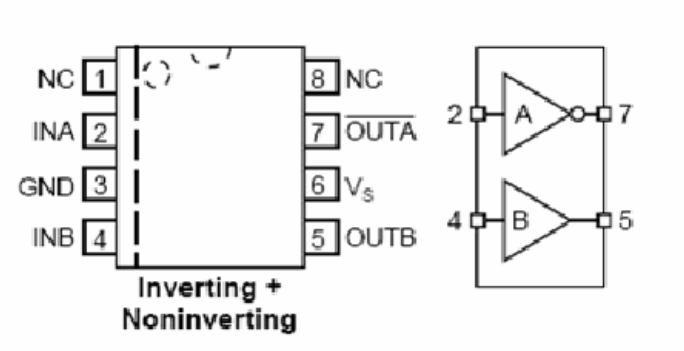
Pin Configuration



Pin Description

Pin Number	Pin Name	Pin Function
1,8	NC	Not internally connected
2	INA	Control input A: TTL/CMOS compatible logic input
3	GND	Ground
4	INB	Control input B: TTL/CMOS compatible logic input
5	OUTB	Output B: CMOS totem-pole output
6	V_S	Supply input: +4.5V to +18V
7	OUTA	Output A: CMOS totem-pole output

Absolute Maximum Ratings (Note 1)

Supply Voltage (V_S)……..……..……..+22V
Input Voltage (V_{IN})……VS +0.3V to GND -5V
Junction Temperature (T_J) ……+150℃
Storage Temperature ……..-65℃ to +150℃
Lead Temperature (10 sec.)……300℃
ESD Rating , Note 3

Operating Ratings (Note 2)

Supply Voltage (V_S)……..+4.5V to +18V
Temperature Range (T_A) ……..-40℃ to +85℃
Package Thermal Resistance
SOIC θ JA ……120℃/W
SOIC θ JC ……75℃/W

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Electrical Characteristics

4.5V≦V_S≦18V; T_A =25℃, bold values indicate full specified temperature range ; unless noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
Input						
V_{IH}	Logic 1 Input Voltage		2.4 2.4	1.4 1.5	- -	V V
V_{IL}	Logic 0 Input Voltage		- -	1.1 1.0	0.8 0.8	V V
I_{IN}	Input	0≦V_{IN}≦V_S	-1	-	1	uA
Output						
V_{OH}	High Output Voltage		VS -0.025	- -	- -	V
V_{OL}	Low Output Voltage		-	-	0.025	V
R_O	Output Resistance	I_{OUT}=10mA, V_S=18V	- -	6 8	10 12	Ω Ω
I_{PK}	Peak Output Current		-	1.5	-	A
I	Latch-Up Protection	With stand reverse current	-	>500	-	mA
Switching Time						
t_R	Rise Time	Test Figure 1	- -	18 20	30 40	ns
t_F	Fall Time	Test Figure 1	- -	15 29	20 40	ns
t_{D1}	Delay Time	Test Figure 1	- -	17 19	30 40	ns
t_{D2}	Delay Time	Test Figure 1	- -	23 27	50 60	ns
t_{PW}	Pulse Time	Test Figure 1	400	-	-	ns
Power Supply						
I_S	Power Supply Current	V_{INA}=V_{INB}=3.0V	- -	1.4 1.5	4.5 8	mA
I_S	Power Supply Current	V_{INA}=V_{INB}=0.0V	- -	0.18 0.19	0.4 0.6	mA

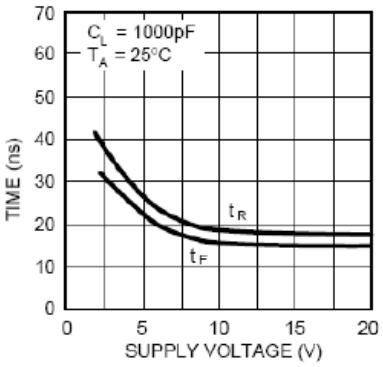
Note 1. Exceeding the absolute maximum rating may damage the device.

Note 2. The device is not guaranteed to function outside its operating rating.

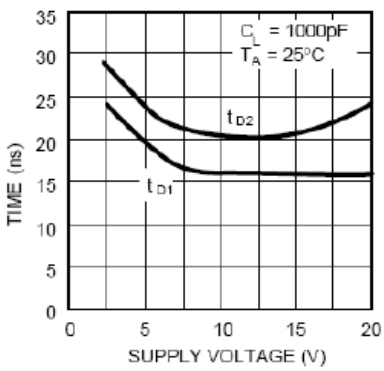
Note 3. Devices are ESD sensitive. Handling precautions recommended.

Electrical Characteristics

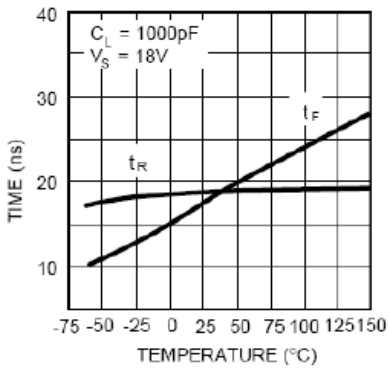
Rise and Fall Time vs. Supply Voltage



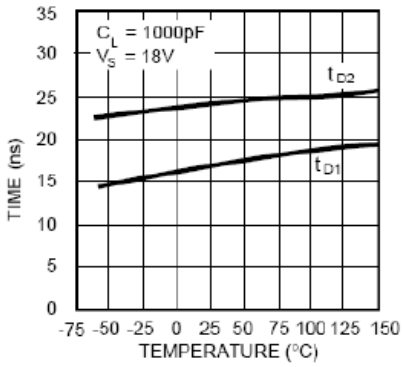
Delay Time vs. Supply Voltage



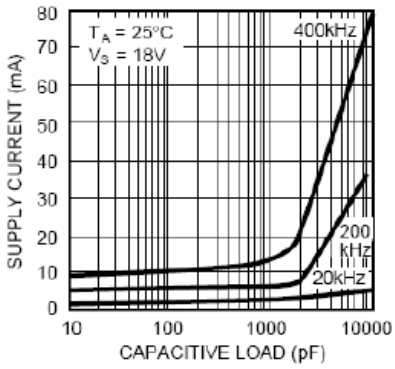
Rise and Fall Time vs. Temperature



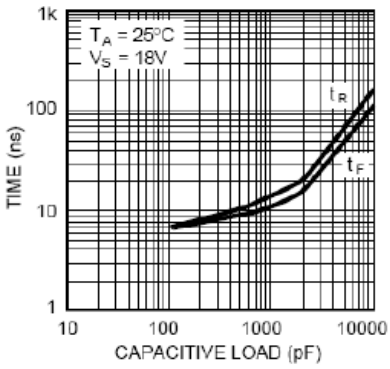
Delay Time vs. Temperature



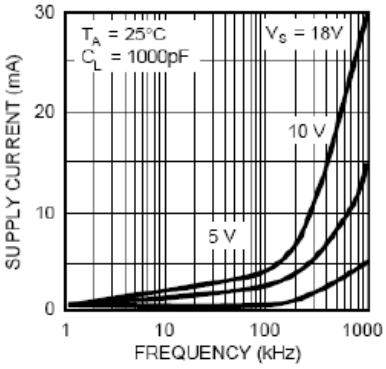
Supply Current vs. Capacitive Load



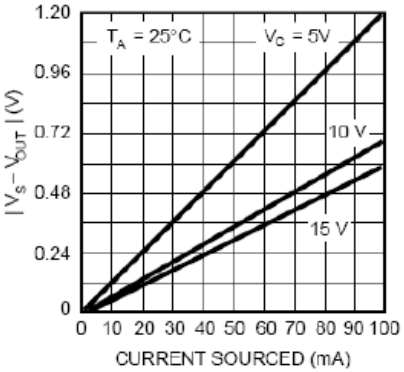
Rise and Fall Time vs. Capacitive Load



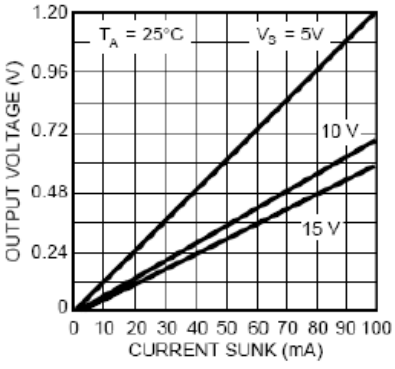
Supply Current vs. Frequency



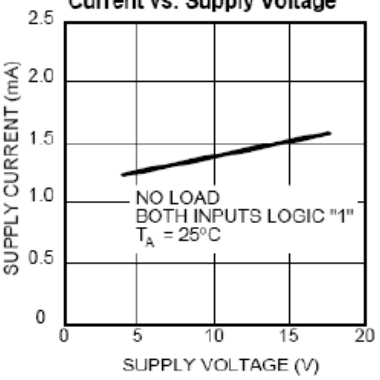
High Output vs. Current



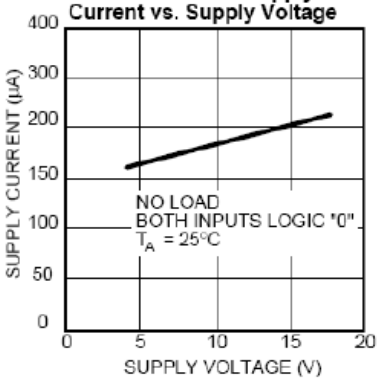
Low Output vs. Current



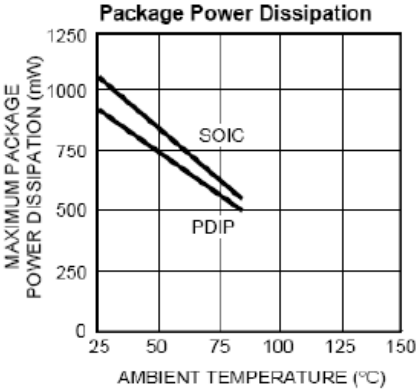
Quiescent Power Supply Current vs. Supply Voltage



Quiescent Power Supply Current vs. Supply Voltage



Package Power Dissipation



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Applications Information

Supply Bypassing

Large currents are required to charge and discharge large capacitive loads quickly. For example, changing a 1000pF load by 16V in 25ns requires 0.8A from the supply input.

To guarantee low supply impedance over a wide frequency range, parallel capacitors are recommended for power supply bypassing. Low-inductance ceramic MLC capacitors with short lead lengths (<0.5”) should be used. A 1.0uF film capacitor in parallel with one or two 0.1uF ceramic MLC capacitors normally provides adequate bypassing.

Grounding

When using the inverting drivers in the TN8118 , individual ground returns for the input and output circuits or a ground plane are recommended for optimum switching speed.

The voltage drop that occurs between the driver’s ground and the input signal ground, during normal high-current switching, will behave as negative feedback and degrade switching speed.

Control Input

Unused driver inputs must be connected to logic high (which can be V_S) or ground. For the lowest quiescent current (<500uA), connect unused inputs to ground. A logic-high signal will cause the driver to draw up to 9mA.

The drivers are designed with 100mV of control input hysteresis. This provides clean transitions and minimizes output stage current spikes when changing states. The control input voltage threshold is approximately 1.5V. The control input recognizes 1.5V up to V_S as a logic high and draws less than 1uA within this range.

Power Dissipation

Power dissipation should be calculated to make sure that the driver is not operated beyond its thermal ratings. Quiescent power dissipation is negligible. A practical value for total power dissipation is the sum of the dissipation caused by the load and the transition power dissipation (P_L+P_T).

Load Dissipation

Power dissipation caused by continuous load current (when driving a resistive load) through the driver’s output resistance is:

$$P_L = I_L^2 R_O$$

For capacitive loads, the dissipation in the driver is:

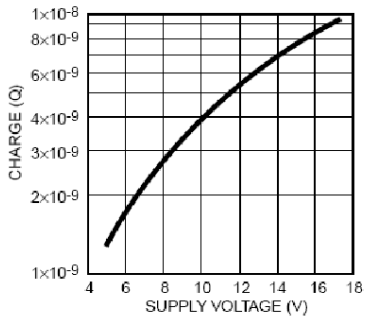
$$P_L = f C_L V_S^2$$

Transition Dissipation

In applications switching at a high frequency, transition power dissipation can be significant. This occurs during switching transitions when the P-channel and N-channel output FETs are both conducting for the brief moment when one is turning on and the other is turning off.

$$P_T = 2fV_SQ$$

Charge (Q) is read from the following graph:



Crossover Energy Loss per Transition

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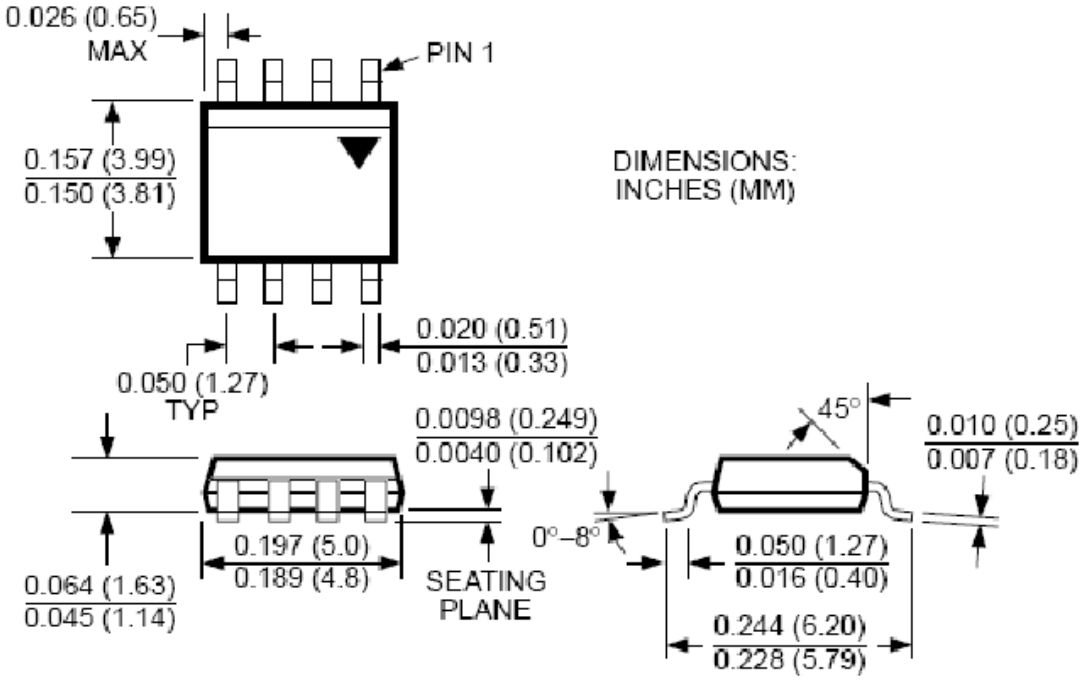
Package Information



8-Lead SOP (M)

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